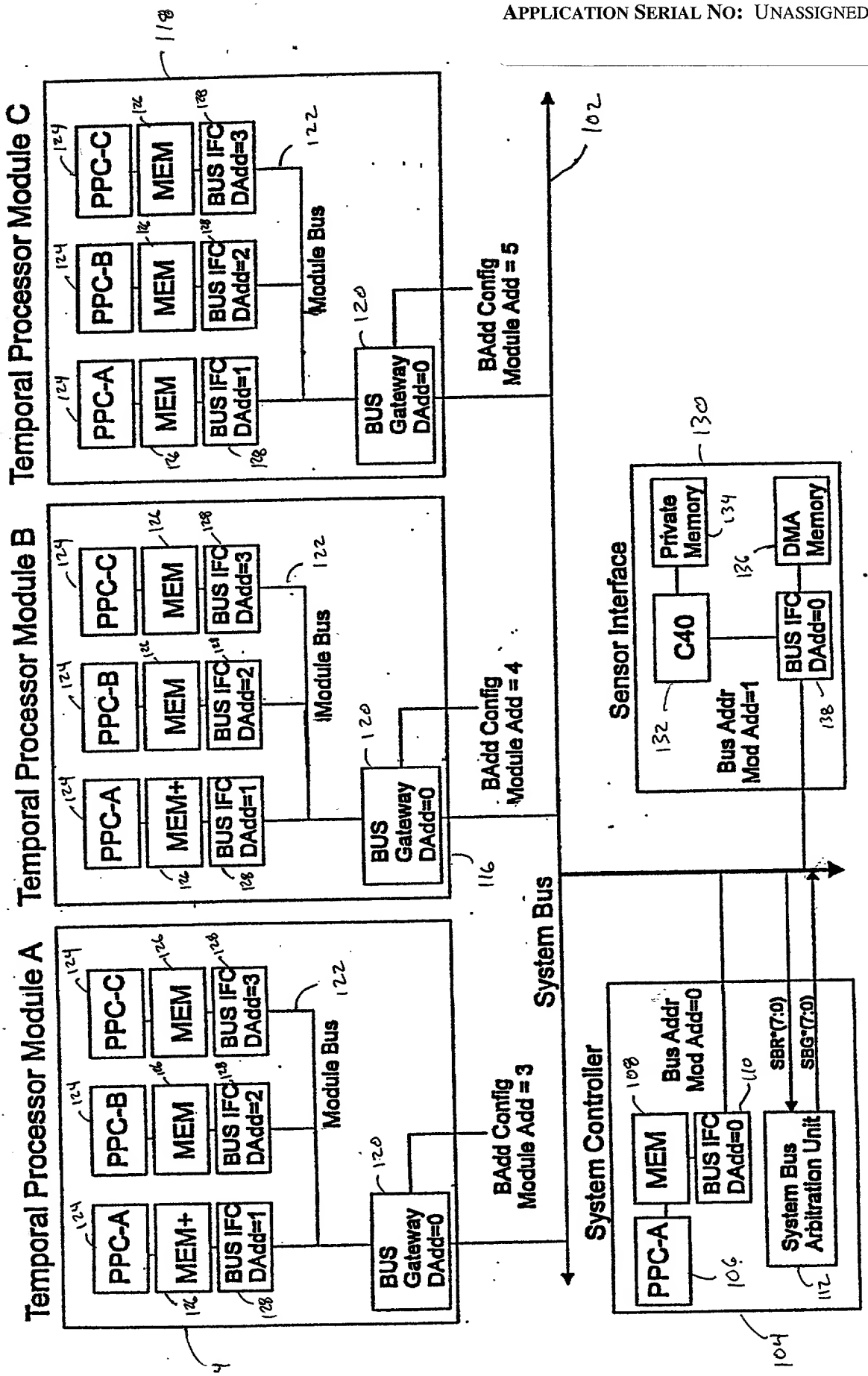
100
Temporal Processor Module A
Temporal Processor Module B
Temporal Processor Module C
PPC-A
PPC-B
PPC-C
MEM
MEM+
BUS IFC DAdd=1
BUS IFC DAdd=2
BUS IFC DAdd=3
BUS Gateway DAdd=0
Module Bus
BAdd Config Module Add = 3
BAdd Config Module Add = 4
BAdd Config Module Add = 5
System Bus
System Controller
Bus Addr Mod Add=0
SBR*(7:0)
SBG*(7:0)
System Bus Arbitration Unit
Sensor Interface
C40
Bus Addr Mod Add=1
Private Memory
DMA Memory
BUS IFC DAdd=0

FIGURE 1

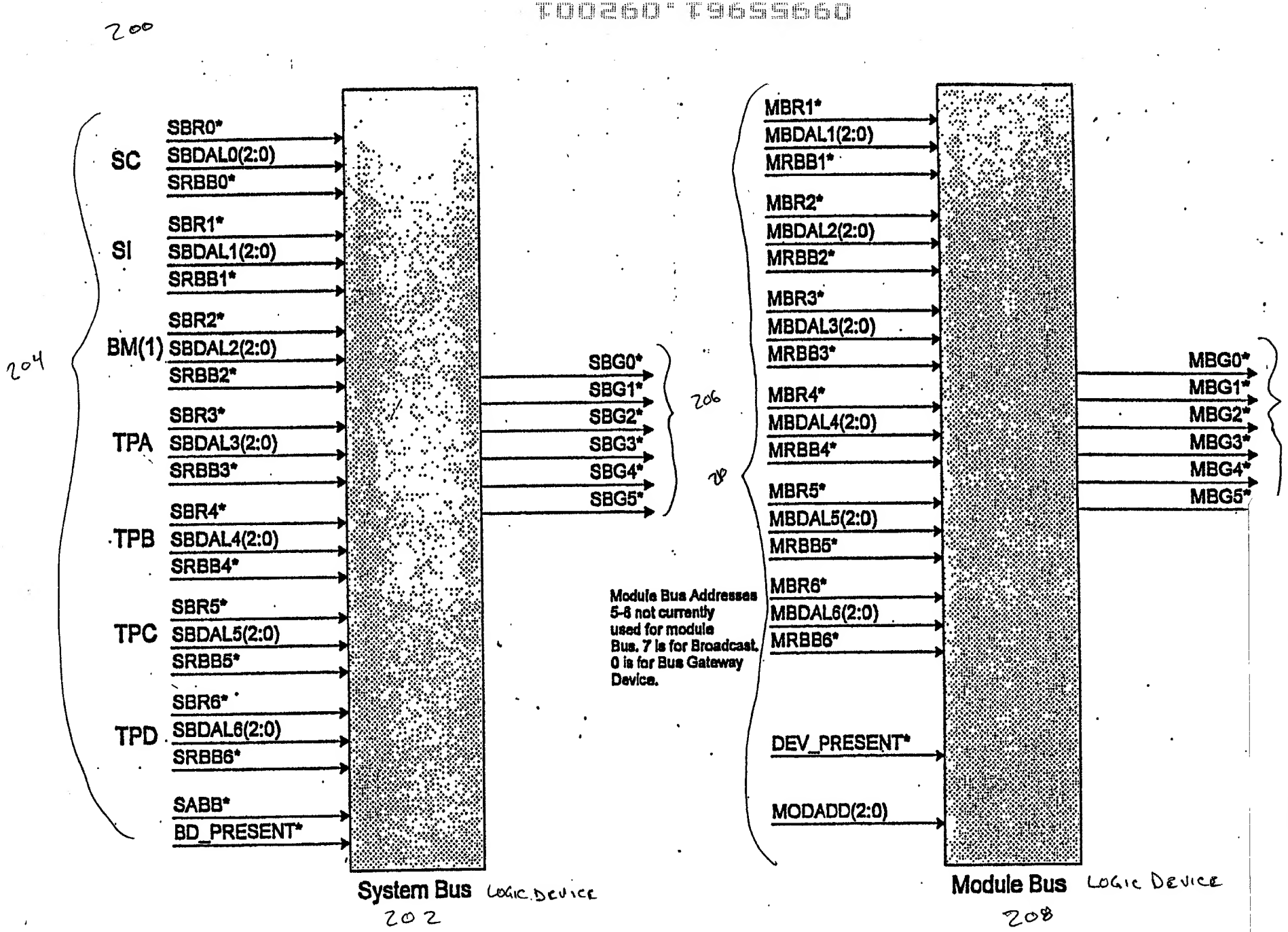

FIGURE 2

APPLN. FILING DATE: SEPTEMBER 20, 2001
TITLE: TWO LEVEL MULTI-TIER SYSTEM BUS
INVENTOR(S): GREGORY S. ANDRE
APPLICATION SERIAL NO: UNASSIGNED

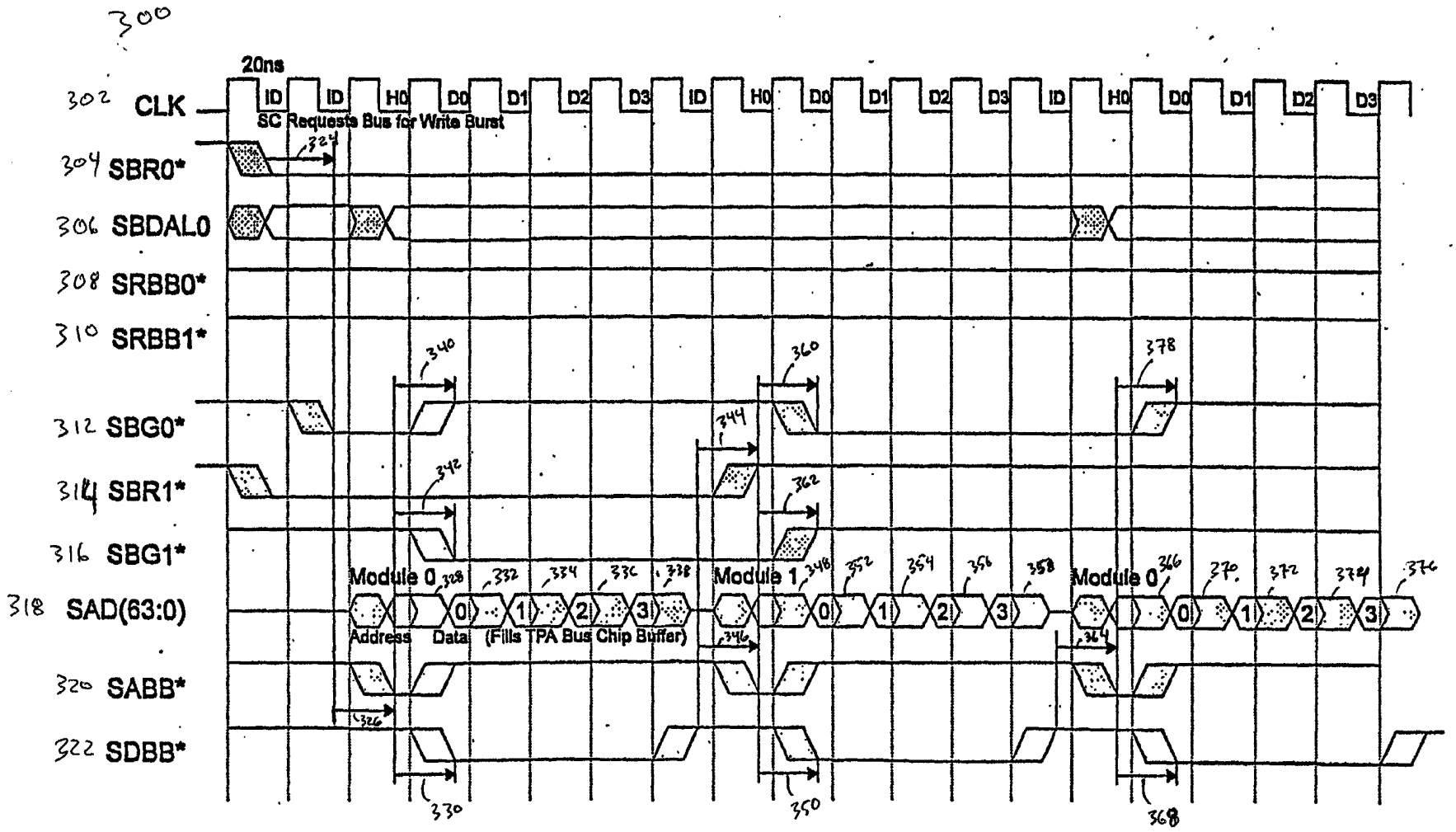
300
20ns
302 CLK
304 SBR0*
306 SBDAL0
308 SRBB0*
310 SRBB1*
312 SBG0*
314 SBR1*
316 SBG1*
318 SAD(63:0)
320 SABB*
322 SDBB*
ID
H0
D0
D1
D2
D3
SC Requests Bus for Write Burst
Module 0
Module 1
Module 0
Address
Data
(Fills TPA Bus Chip Buffer)

FIGURE 3

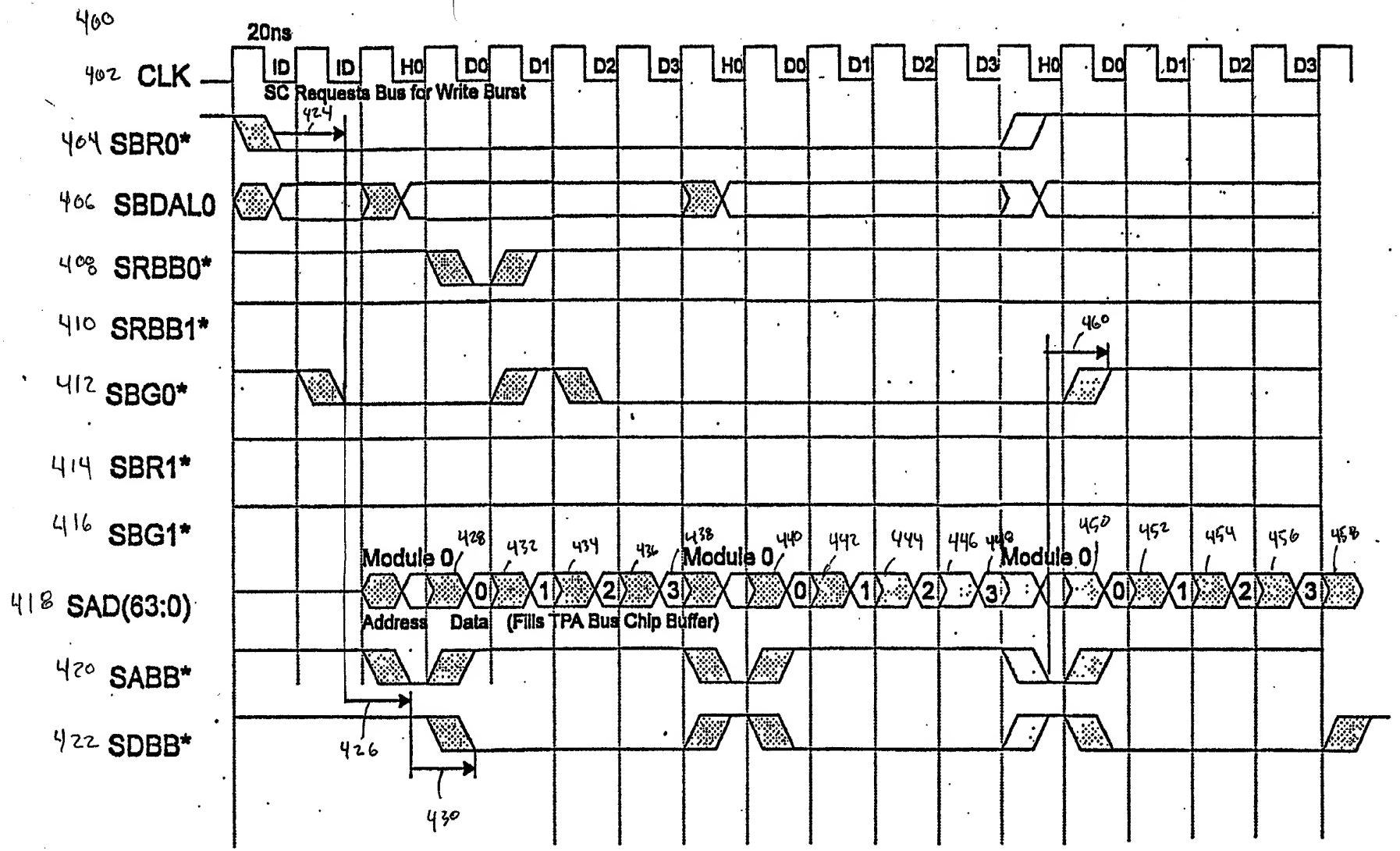
400
20ns
402 CLK
ID
ID
H0
D0
D1
D2
D3
SC Requests Bus for Write Burst
424
404 SBR0*
406 SBDAL0
408 SRBB0*
410 SRBB1*
460
412 SBG0*
414 SBR1*
416 SBG1*
Module 0
428
432
434
436
Module 0
440
442
444
446
448
Module 0
450
452
454
456
458
418 SAD(63:0)
Address
Data
(Fills TPA Bus Chip Buffer)
420 SABB*
422 SDBB*
426
430

FIGURE 4

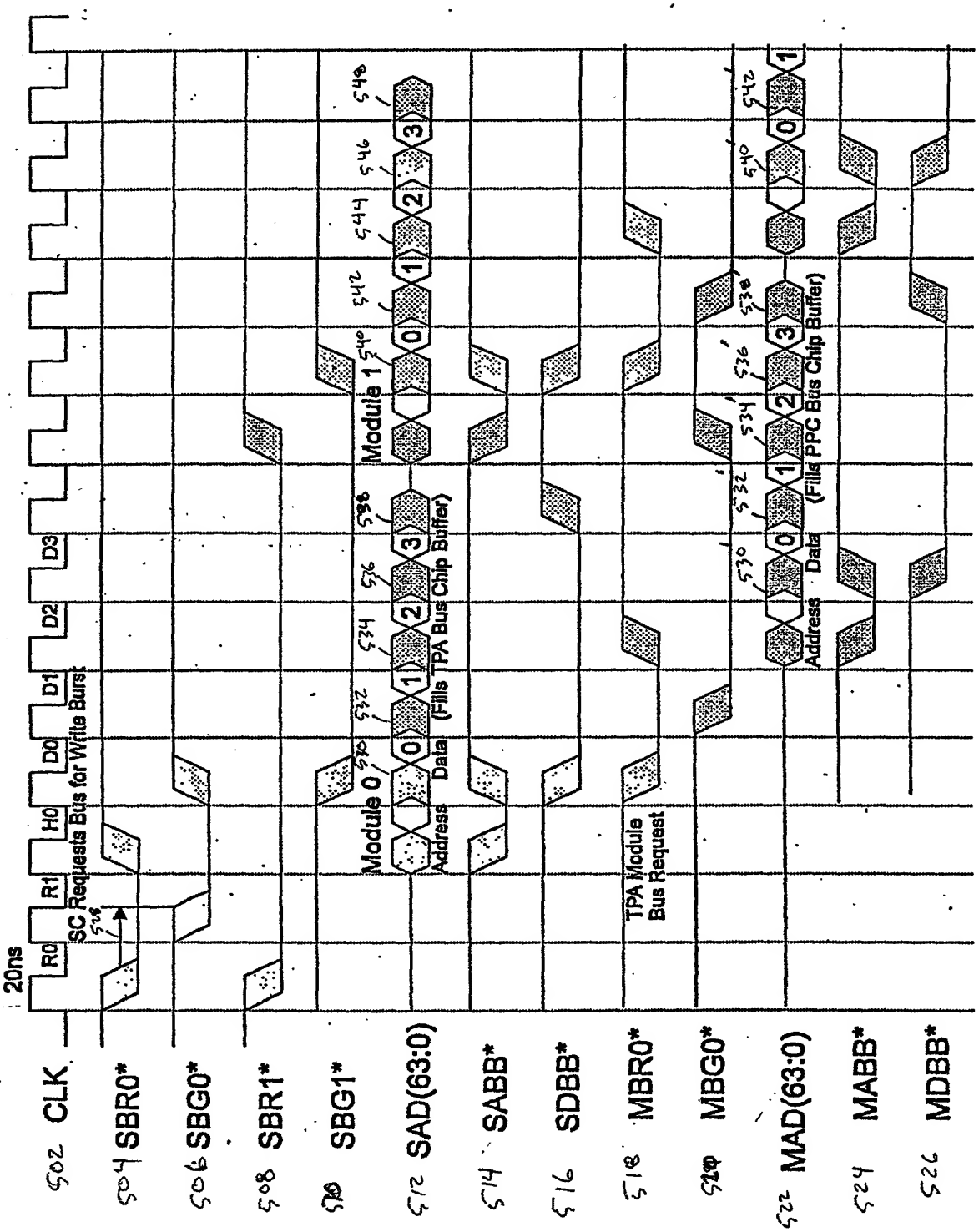
20ns
R0
R1
H0
D0
D1
D2
D3
SC Requests Bus for Write Burst
TPA Module Bus Request
Module 0 Address
Data (Fills TPA Bus Chip Buffer)
Module 1 Address
Data (Fills PPC Bus Chip Buffer)
502 CLK
504 SBR0*
506 SBG0*
508 SBR1*
510 SBG1*
512 SAD(63:0)
514 SABB*
516 SDBB*
518 MBR0*
520 MBG0*
522 MAD(63:0)
524 MABB*
526 MDBB*

FIGURE 5

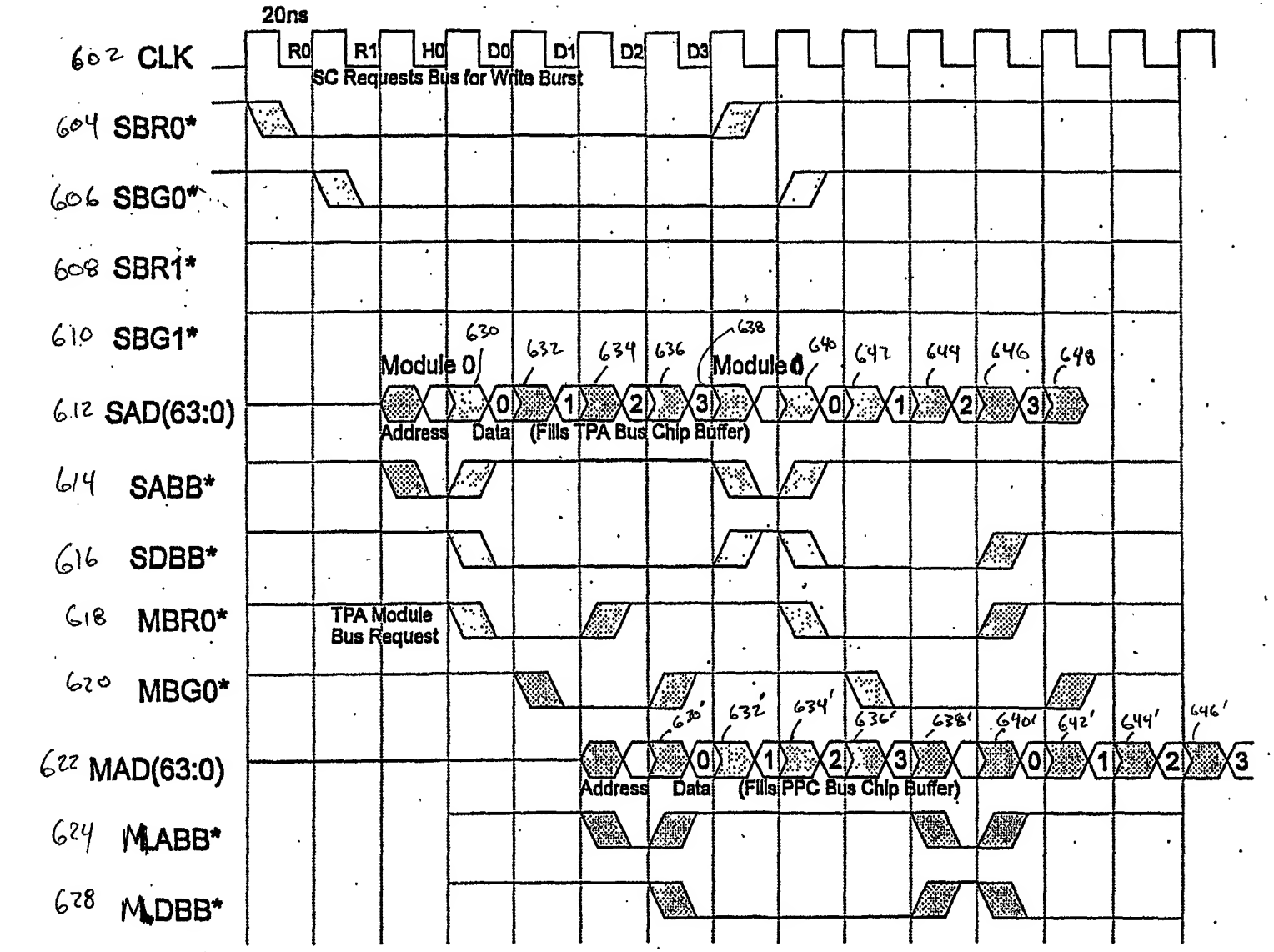
600
20ns
602 CLK
R0
R1
H0
D0
D1
D2
D3
SC Requests Bus for Write Burst
604 SBR0*
606 SBG0*
608 SBR1*
610 SBG1*
612 SAD(63:0)
Module 0
Module 0
630
632
634
636
638
640
642
644
646
648
Address
Data
(Fills TPA Bus Chip Buffer)
614 SABB*
616 SDBB*
618 MBR0*
TPA Module Bus Request
620 MBG0*
622 MAD(63:0)
630'
632'
634'
636'
638'
640'
642'
644'
646'
Address
Data
(Fills PPC Bus Chip Buffer)
624 MABB*
628 MDBB*

FIGURE 6

700

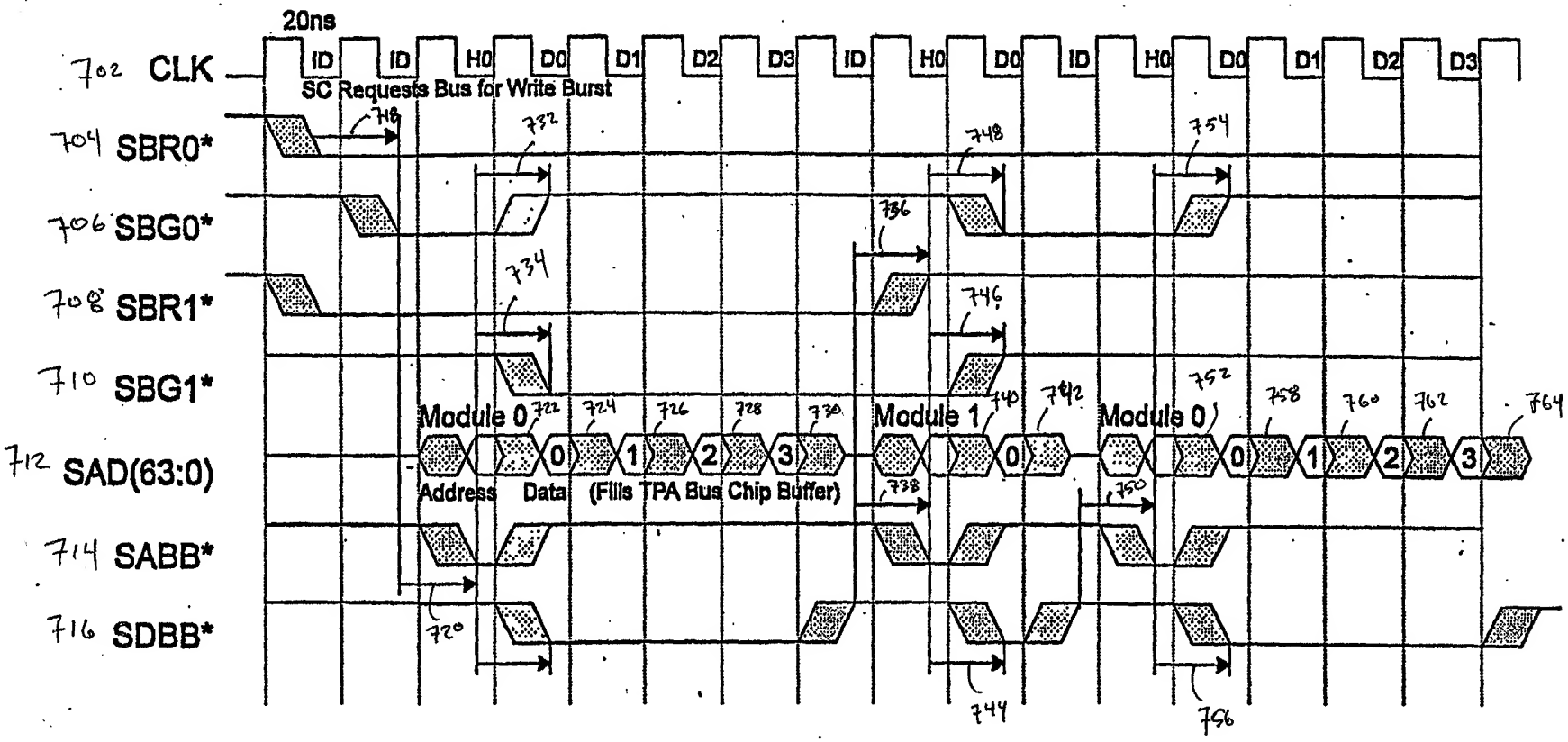
20ns
702 CLK
704 SBR0*
706 SBG0*
708 SBR1*
710 SBG1*
712 SAD(63:0)
714 SABB*
716 SDBB*
ID
H0
D0
D1
D2
D3
SC Requests Bus for Write Burst
Module 0
Module 1
Module 0
Address
Data
(Fills TPA Bus Chip Buffer)
718
720
722
724
726
728
730
732
734
736
738
740
742
744
746
748
750
752
754
756
758
760
762
764

FIGURE 7

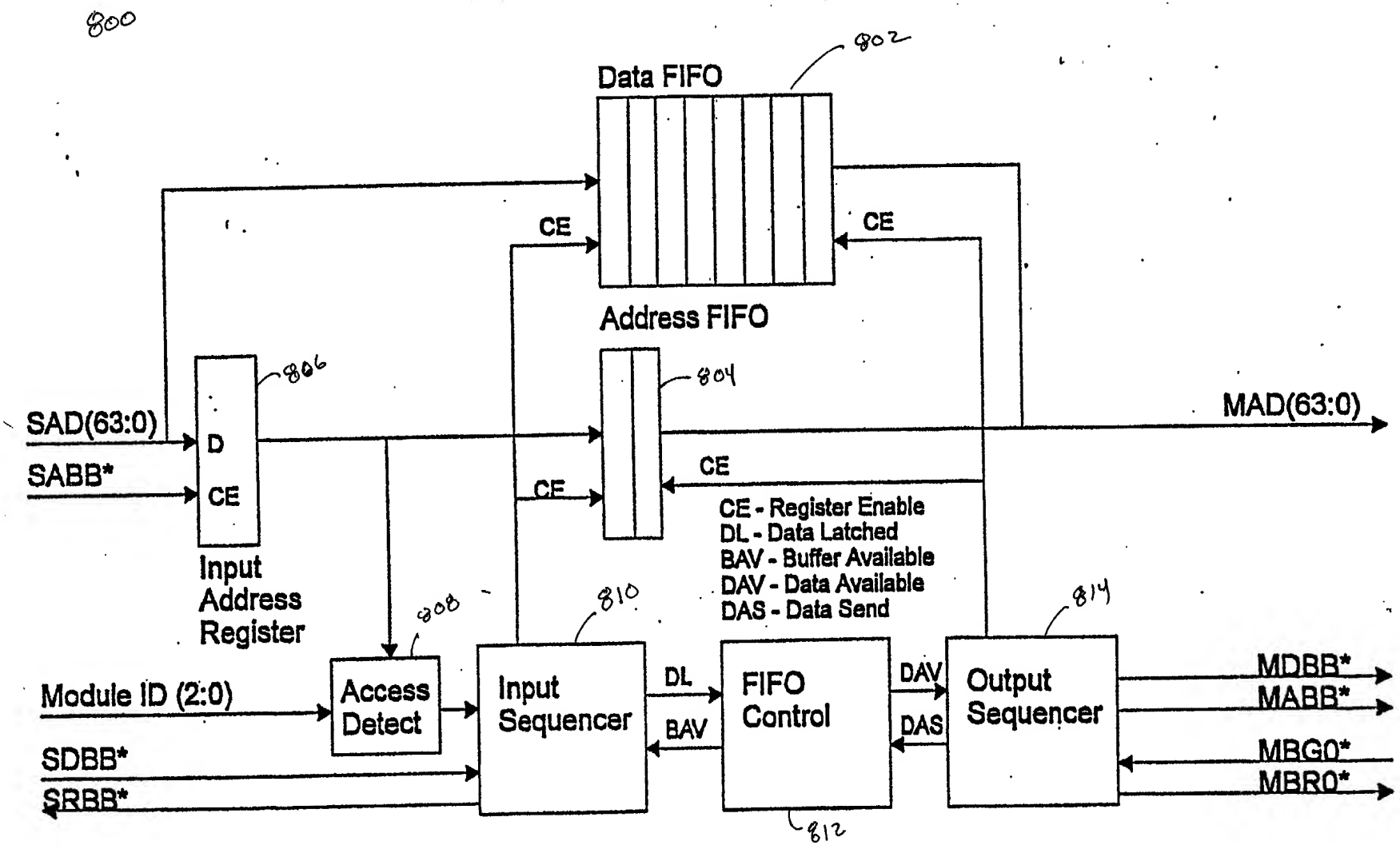
800
Data FIFO
802
CE
CE
Address FIFO
804
806
SAD(63:0)
SABB*
D
CE
MAD(63:0)
CE
CE
CE - Register Enable
DL - Data Latched
BAV - Buffer Available
DAV - Data Available
DAS - Data Send
Input
Address
Register
808
810
814
Module ID (2:0)
Access
Detect
Input
Sequencer
DL
BAV
FIFO
Control
DAV
DAS
Output
Sequencer
MDBB*
MABB*
MBG0*
MBR0*
SDBB*
SRBB*
812

FIGURE 8

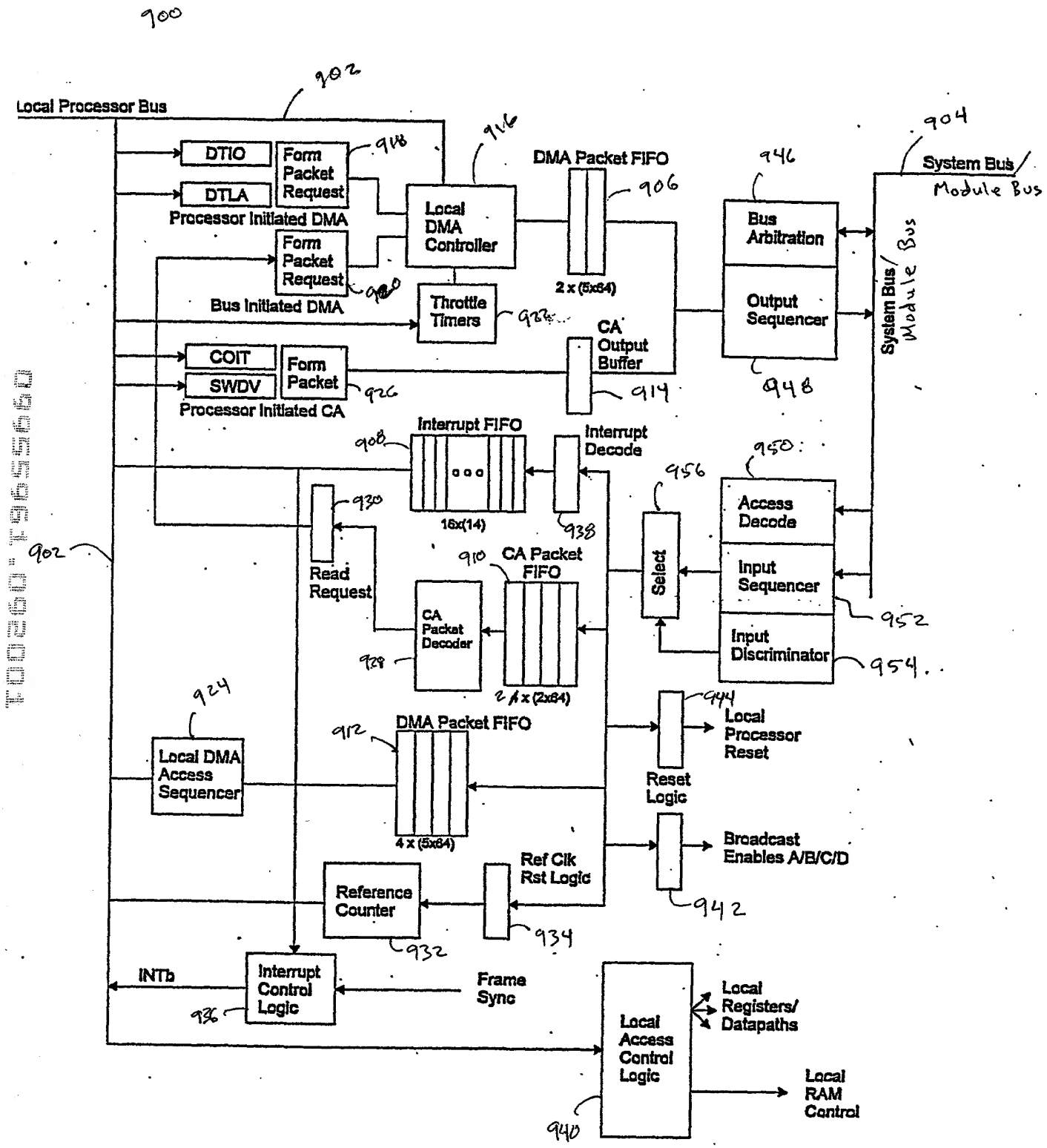
900
902
Local Processor Bus
DTIO
DTLA
Processor Initiated DMA
Form Packet Request
918
Form Packet Request
Bus Initiated DMA
Local DMA Controller
916
DMA Packet FIFO
906
2 x (5x64)
Throttle Timers
928
CA Output Buffer
914
COIT
SWDV
Processor Initiated CA
Form Packet
926
Interrupt FIFO
908
16x(14)
Interrupt Decode
938
930
Read Request
910
CA Packet FIFO
CA Packet Decoder
928
2 x (2x64)
924
Local DMA Access Sequencer
912
DMA Packet FIFO
4 x (5x64)
Ref Clk Rst Logic
Reference Counter
932
934
INTb
Interrupt Control Logic
936
Frame Sync
Local Access Control Logic
940
Local Registers/ Datapaths
Local RAM Control
946
Bus Arbitration
Output Sequencer
948
904
System Bus / Module Bus
950
956
Access Decode
Select
Input Sequencer
952
Input Discriminator
954
944
Local Processor Reset
Reset Logic
Broadcast Enables A/B/C/D
942

FIGURE 9

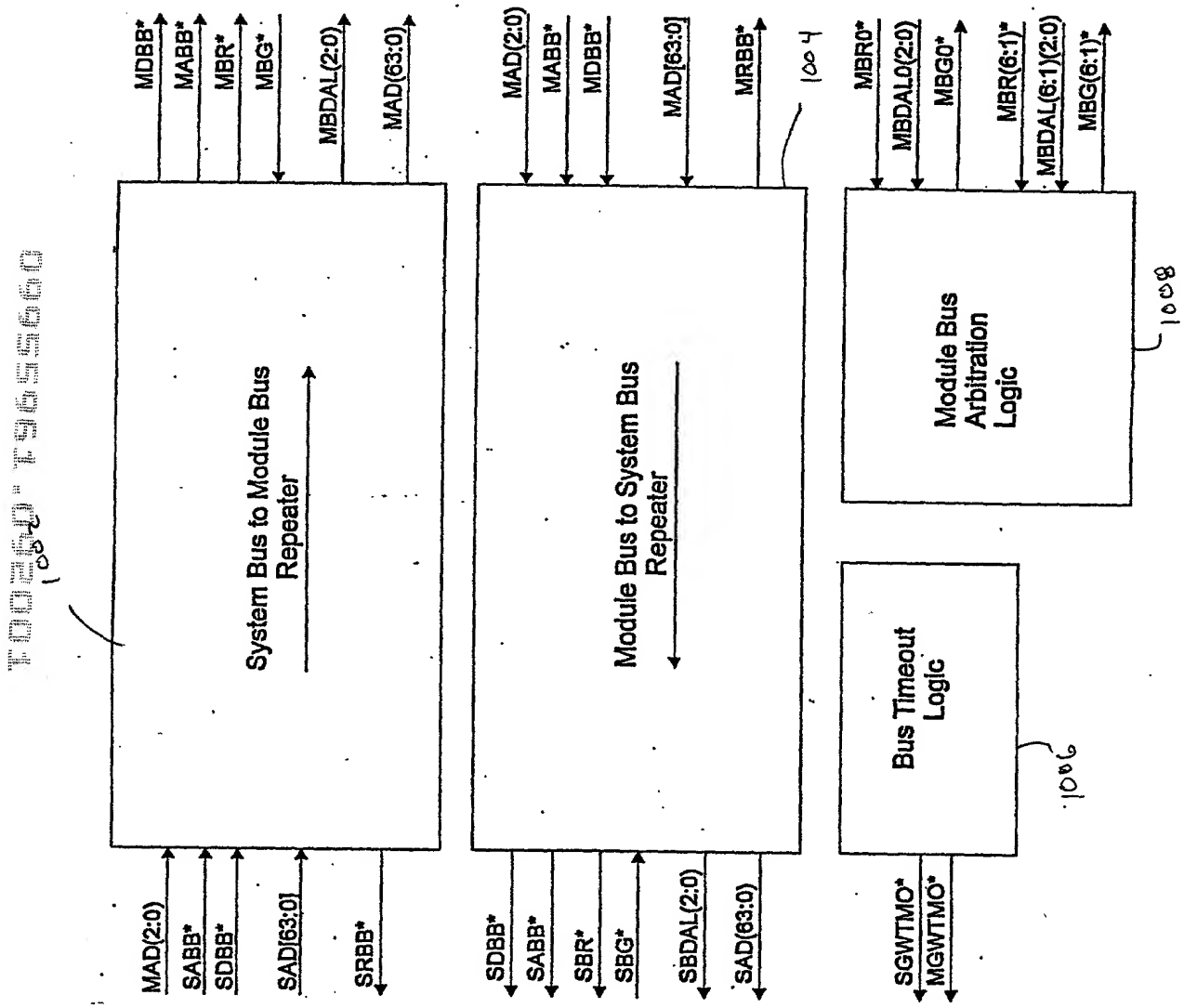
MDBB*
MABB*
MBR*
MBG*
MBDAL(2:0)
MAD(63:0)
System Bus to Module Bus Repeater
1002
MAD(2:0)
SABB*
SDBB*
SAD(63:0)
SRBB*
MAD(2:0)
MABB*
MDBB*
MAD[63:0]
MRBB*
Module Bus to System Bus Repeater
1004
SDBB*
SABB*
SBR*
SBG*
SBDAL(2:0)
SAD(63:0)
MBR0*
MBDAL0(2:0)
MBG0*
MBR(6:1)*
MBDAL(6:1)(2:0)
MBG(6:1)*
Module Bus Arbitration Logic
1008
Bus Timeout Logic
1006
SGWTMO*
MGWTMO*
1000

FIGURE 10

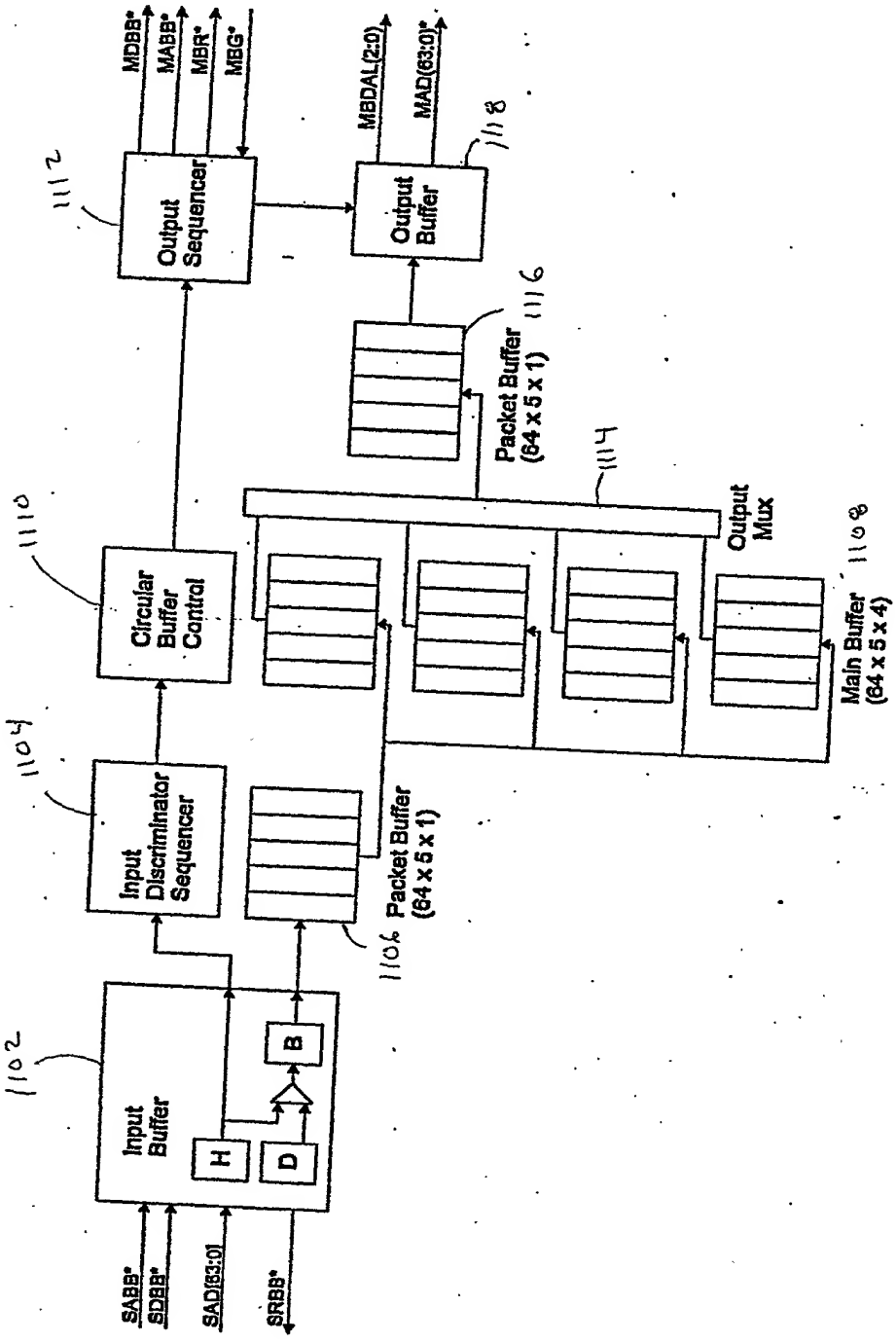
MDBB*
MABB*
MBR*
MBG*
MBIDAL(2:0)
MAD(63:0)*
1118
1112
Output Sequencer
Output Buffer
1116
Packet Buffer (64 x 5 x 1)
1114
Output Mux
1110
Circular Buffer Control
1108
Main Buffer (64 x 5 x 4)
1104
Input Discriminator Sequencer
1106
Packet Buffer (64 x 5 x 1)
1102
Input Buffer
B
H
D
SABB*
SDBB*
SAD(63:0)
SRBB*
1100

FIGURE 11

1200

~~Fig. 10~~

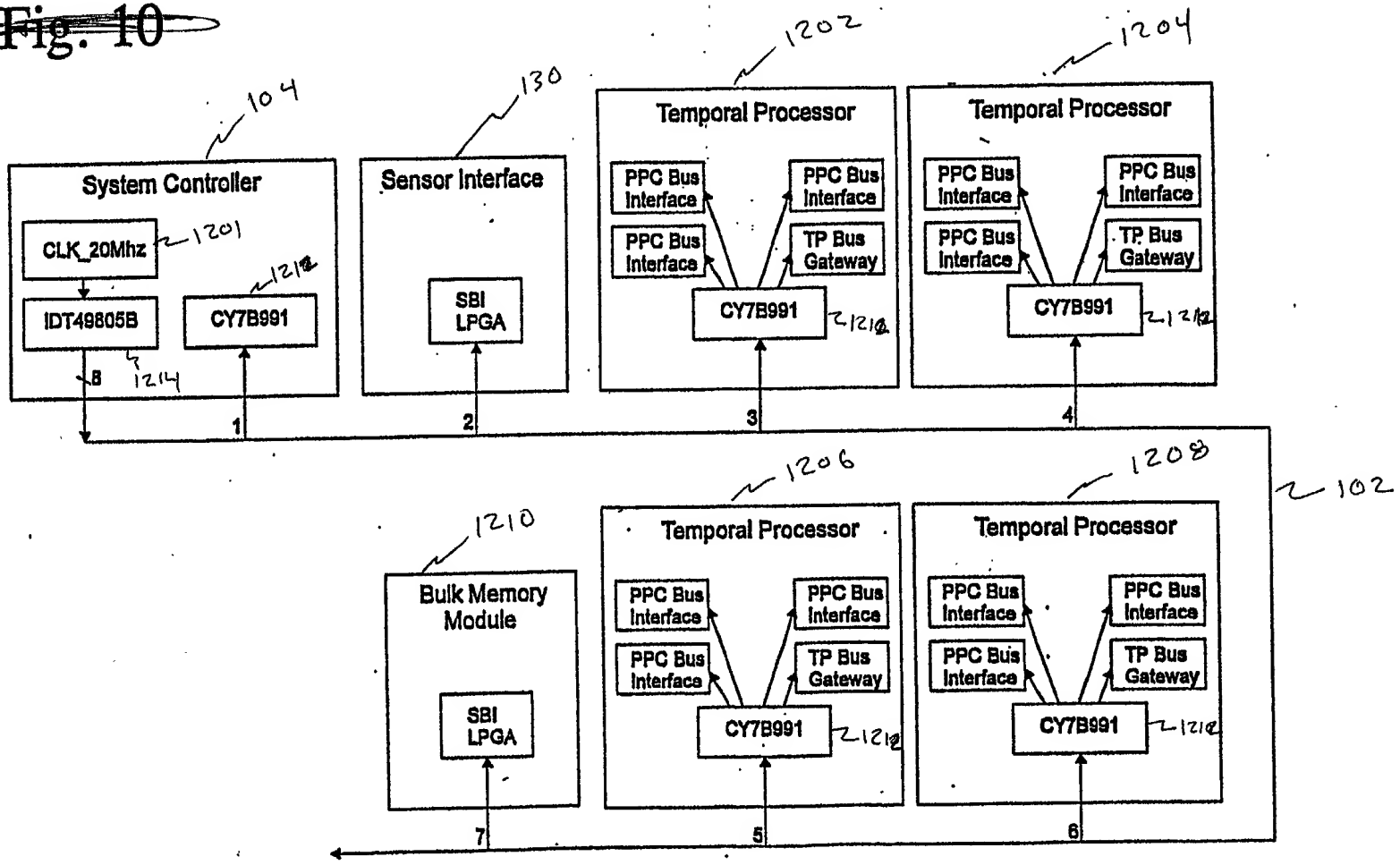

FIGURE 12